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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/004,002	11/30/2001	Gilroy J. Vandentop	884.540US1	5879

7590 04/03/2003

Schwegman, Lundberg, Woessner & Kluth, P.A.
P.O. Box 2938
Minneapolls, MN 55402

EXAMINER
VIGUSHIN, JOHN B

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 04/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/004,002	VANDENTOP ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,9-13,15-18,20,21,27,31,32,34-36,39 and 42* is/are rejected.

7)☒ Claim(s) *3,6-8,14,19,22-26,28-30,33,37,38,40 and 41* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Rejections Based On Prior Art

1. The following references were relied upon for the rejections hereinbelow:

Dockerty et al. (US 6,053,394) Dockerty et al. (US 5,796,169)

Grieco et al. (US 5,758,099) Hernandez* et al. (US 5,309,324)

Lin et al. (US 5,239,198) Zifcak et al. (US 4,793,814)

*The patent cites "Herandez" as co-inventor. This is a misprint. The correct name is Hernandez.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.0

3. Claims 1, 2, 4, 5, 9, 10, 12, 13, 17, 18, 20, 21, 27, 31 and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Dockerty et al. **(US 5,796,169)**.

As to Claim 1, Dockerty et al. discloses aligning first and second sets of terminals 4 and 15, respectively, of an IC die 3 (Fig. 4; col.3: 23-26; col.4: 36-38) with corresponding third and fourth sets of terminals 2 and 34, respectively, of a substrate (said substrate not shown but similar to substrate 1 in the IC package mounting embodiment of Fig. 5), the first and second sets of terminals 4 and 15 being in first and second zones (second zone is labeled as 14), respectively, of IC 3 (Figs. 3 and 4);

coupling the first and third sets of terminals 4 and 2 with a first type of connector 11; coupling the second and fourth sets of terminals 15 and 34 with a second type of connector 16, 18 (Figs. 3 and 4; the coupling of IC 3 to a substrate is not shown but is similar to the coupling of IC package 24--having the same layout as IC 3--to substrate 1 in Fig. 5).

As to Claim 2, Dockerty et al. further discloses forming the first and second sets of terminals 4 and 15 on a surface of the IC 3 (Fig. 4).

As to Claim 4, Dockerty et al. further discloses forming the second zone 14 in a peripheral region of the surface (Fig. 3).

As to Claim 5, Dockerty et al. further discloses coupling the first and third sets of terminals 4 and 2 with the first type of connector 11 comprises using solder (not shown but similar to the IC package 24 coupling to substrate 1 shown in Fig. 5; col.4: 56-63).

As to Claim 9, Dockerty et al. discloses aligning first and second sets of terminals (attached respectively to connectors 11 and 33) of an IC package 24 (col.5: 28-30) with corresponding third and fourth sets of terminals 2 and 34, respectively, of a substrate 1, the first and second terminals being in first and second zones, respectively, of the IC package 24 (said zones not explicitly shown but similar to the zones defined by the configuration in the IC die embodiment of Fig. 3; col.5: 38-48); coupling the first and third sets of terminals with a first type of connector 11 (Fig. 5); and coupling the second and fourth sets of terminals with a second type of connector 33 (Fig. 5; col.5: 38-48).

As to Claim 10, Dockerty et al. further discloses forming the first and second sets of terminals on a surface of IC package 24 (Fig. 5).

As to Claim 12, Dockerty et al. further discloses forming the second zone in a peripheral region (col.5: 41-48; compare with zone 14 of the IC die in Fig. 3).

As to Claim 13, Dockerty et al. further discloses that coupling the first and third sets of terminals with the first type of connector 11 comprises using solder (col.5: 38-41).

As to Claim 17, Dockerty et al. discloses a die 3 (Fig. 4; col.3: 23-26; col.4: 36-38) comprising first and second sets of terminals 4 and 15 disposed in first and second zones (second zone is labeled as 14), respectively, of the die 3 (Figs. 3 and 4); a substrate comprising third and fourth sets of terminals 2 and 34, respectively, of a substrate (said substrate not shown but having connector configuration similar to that of substrate 1 in the IC package mounting embodiment of Fig. 5); a first type of connector 11 to couple the first and third sets of terminals 4 and 2; and a second type of connector 16, 18 to couple the second and fourth sets of terminals 15 and 34 (Figs. 3 and 4; the coupling of IC 3 to a substrate is not shown but is similar to the coupling of IC package 24--having the same type of connector configuration as IC 3--to substrate 1 in Fig. 5).

As to Claim 18, Dockerty et al. further discloses that the first and second sets of terminals 4 and 15 are disposed on a surface of die 3 (Fig. 4).

As to Claim 20, Dockerty et al. further discloses that the second zone 14 is peripherally located on the surface (Fig. 3).

As to Claim 21, Dockerty et al. further discloses that the first type of connector 11 comprises solder (col.4: 56-63).

As to Claim 27, Dockerty et al. discloses that die 3 further comprises a fifth set of terminals 15 disposed in a third zone 22 of die 3, wherein the substrate comprises a sixth set of terminals 34 (said substrate not shown but having connector configuration similar to that of substrate 1 in the IC package mounting embodiment of Fig. 5); a third type of connector 23 to couple the fifth and sixth sets of terminals (Fig. 3).

As to Claim 31, Dockerty et al. discloses an IC package 24 (col.5: 28-30) comprising first and second sets of terminals (attached respectively to connectors 11 and 33) disposed in first and second zones, respectively, of a surface of IC package 24 (Fig. 5; said zones not shown but compare with the zones of Fig. 3 defined by connectors 11 and 16, 18 and similar to said zones of IC package 24; col.5: 38-48); a substrate 1 comprising third and fourth sets of terminals 2 and 34, respectively (Fig. 5); a first type of connector 11 to couple the first and third sets of terminals (Fig. 5); a second type of connector 33 to couple the second and fourth sets of terminals (Fig. 5; col.5: 41-48).

As to Claim 36, Dockerty et al. discloses a die 3 (Fig. 4; col.3: 23-26; col.4: 36-38) comprising first and second sets of terminals 4 and 15 disposed in first and second zones (second zone is labeled as 14), respectively, of a surface of die 3 (Figs. 3 and 4); a substrate comprising third and fourth sets of terminals 2 and 34, respectively, of a substrate (said substrate not shown but having connector configuration similar to that of substrate 1 in the IC package mounting embodiment of Fig. 5); a first type of connector 11 to couple the first and third sets of terminals 4 and 2; and a second type of connector 16, 18 to couple the second and fourth sets of terminals 15 and 34 (Figs. 3 and 4; the

coupling of IC 3 to a substrate is not shown but is similar to the coupling of IC package 24--having the same type of connector configuration as IC 3--to substrate 1 in Fig. 5).

4. Claims 9-13, 31 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin et al.

As to Claim 9, Lin et al. discloses aligning first and second sets of terminals 42 and 44, respectively, of an IC circuit package 10 with corresponding third and fourth terminals 40 of a substrate 38 (Figs. 4 and 5; col.6: 33-35 and 36-38; col.5: 63-67), the first and second sets of terminals 42 and 44 being in first and second zones, respectively, of the IC package (Fig. 5); coupling the first set of terminals 42 and third set of terminals 40 with a first type of connector 32 (Fig. 4; col.6: 35-36 and col.5: 63-67); and coupling the second set of terminals 44 and fourth set of terminals 40 with a second type of connector 36 (Fig. 4; col.6: 39-42 and col.5: 63-67).

As to Claim 10, Lin et al. further discloses forming the first and second sets of terminals 42 and 44 on a surface (i.e., the bottom surface) of IC package 10 (Fig. 5).

As to Claim 11, Lin et al. further discloses forming the first zone (wherein first set of terminals 42 is located) in a central region of the surface (Fig. 5).

As to Claim 12, Lin et al. further discloses forming the second zone (wherein second set of terminals 44 is located) in a peripheral region of the surface (Fig. 5).

As to Claim 13, Lin et al. further discloses that coupling the first and third sets of terminals 42 and 40, respectively, with the first type of connector 32 comprises solder (Fig. 4; col.6: 35-36).

As to Claim 31, Lin et al. discloses an IC package 10 comprising first and second sets of terminals 42 and 44 disposed in first and second zones, respectively, of a surface (i.e., the bottom surface) of IC package 10 (Figs. 4 and 5; col.6: 33-35 and 36-38); a substrate 38 comprising third and fourth sets of terminals 40 (Fig. 4; col.5: 63-67); a first type of connector 32 to couple the first set of terminals 42 and third set of terminals 40 (Fig. 4; col.6: 35-36 and col.5: 63-67); and a second type of connector 36 to couple the second set of terminals 44 and fourth set of terminals 40 (Fig. 4; col.6: 39-42 and col.5: 63-67).

As to Claim 32, Lin et al. further disclose that the first zone (corresponding to terminal set 42) is centrally located on the IC surface (Fig. 5), and the first type of connector 32 comprises solder (col.6: 35-36).

5. Claims 9-13, 16, 31 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Dockerty et al **(US 6,053,394)**.

As to Claim 9, Dockerty et al. discloses aligning first and second sets of terminals 3 and 13, respectively, of an IC package 1 with corresponding third and fourth sets of terminals 4 and 16, respectively, of a substrate 6, the first and second sets of terminals 3 and 13 being in first and second zones, respectively, of the IC package (Fig. 2; col.4: 41-45); coupling the first and third sets of terminals 3 and 4 with a first type of connector 7 (Figs. 2 and 3); and coupling the second and fourth sets of terminals 13 and 16 with a second type of connector 14 (Figs. 2 and 3; col.4: 38-58; col.5: 52-56).

As to Claim 10, Dockerty et al. further discloses forming the first and second sets of terminals 3 and 13 o a surface of IC package 1 (Fig. 2).

As to Claim 11, Dockerty et al. further discloses forming the first zone (wherein first set of terminals 3 is located) in a central region of the surface (Fig. 3).

As to Claim 12, Dockerty et al. further discloses forming the second zone (wherein second set of terminals 13 is located) in a peripheral region (Fig. 3; col.4: 41-45).

As to Claim 13, Dockerty et al. further discloses that coupling the first and third sets of terminals with the first type of connector 7 comprising solder (col.4: 38-41).

As to Claim 16, Dockerty et al. further discloses that coupling the second and fourth sets of terminals with the second type of connector comprises physically compressing the IC package 1 and substrate 6 together by means of spring 8 (col.4: 27-37; col.4: 62-65).

As to Claim 31, Dockerty et al. discloses an IC package 1 comprising first and second sets of terminals 3 and 13 disposed in first and second zones, respectively, of a surface of the IC package (Fig. 2; col.4: 41-45); a substrate 6 comprising third and fourth sets of terminals 4 and 16, respectively (Fig. 2); a first type of connector 7 to couple the first and third sets of terminals 3 and 4 (Figs. 2 and 3); and a second type of connector 14 to couple the second and fourth sets of terminals 13 and 16 (Figs. 2 and 3; col.4: 38-58; col.5: 52-56).

As to Claim 32, Dockerty et al. further discloses that the first zone is centrally located on the surface, and the first type of connector 7 comprises solder (Fig. 3; col.4: 38-41).

6. Claims 9-13, 15, 16, 31, 32, 34 and 35 are rejected under 35 U.S.C. 102(b) as being anticipated by Hernandez et al.

As to Claim 9 (*Rejection #1*): Hernandez et al. discloses aligning first and second sets of terminals 136 and 16, respectively, of an IC package 10 with corresponding third and fourth sets of terminals 140 and 42 of a substrate 12, the first and second sets of terminals 136 and 16 being in first and second zones--wherein first zone is labeled with element number 20--, respectively, of IC package 10 (Figs. 1, 1A and 12; col.5: 42-43; col.9: 19-23); coupling the first and third sets of terminals 136 and 140 with a first type of connector (Fig. 12; col.9: 19-26); and coupling the second and fourth sets of terminals 16 and 42 on a surface of IC package 10 (Figs. 1 and 12; col.6: 4-14 and 19-25).

As to Claim 9 (*Rejection #2*): Hernandez et al. discloses aligning first and second sets of terminals 136 and 16, respectively, of an IC package 10 with corresponding third and fourth sets of terminals 142/144 (via feed holes 142 in conjunction with associated vias 144; col.9: 24-26) and 42, respectively (Figs. 1 and 12; col.5: 64-66; col.9: 24-30) of a substrate 12, the first and second sets of terminals 136 and 16 being in first and second zones--wherein first zone is labeled with element number 20--, respectively, of IC package 10 (Figs. 1, 1A and 12; col.5: 42-43; col.9: 19-23); coupling the first and third sets of terminals 136 and 142/144 with a first type of connector 134/140 (pins 134 in conjunction with associated sockets 140; col.9: 24-28); and coupling the second and fourth sets of terminals 16 and 42 on a surface of IC package 10 (Figs. 1 and 12; col.6: 4-14 and 19-25).

As to Claim 10 (depending from either one of *Rejection #1* and *Rejection #2* of base Claim 9, above), Hernandez et al. further discloses forming the first and second sets of terminals 136 and 16 on a surface 18 of IC package 10 (Fig. 12).

As to Claim 11 (depending from either one of *Rejection #1* and *Rejection #2* of base Claim 9, above), Hernandez et al. further discloses forming the first zone 20 in a central region of surface 18 (Figs. 1A and 12).

As to Claim 12 (depending from either one of *Rejection #1* and *Rejection #2* of base Claim 9, above), Hernandez et al. further discloses forming the second zone (wherein second set of terminals 16 is located) in a peripheral region of surface 18 (Figs. 1A and 12).

As to Claim 13 (depending from *Rejection #2* of base Claim 9, above), Hernandez et al. further discloses that coupling the first and third sets of terminals 136 and 142/144 with the first type of connector 134/140 comprises using solder (Figs. 1A and 12; col.9: 27-30).

As to Claim 15 (depending from either one of *Rejection #1* and *Rejection #2* of base Claim 9, above), Hernandez et al. further discloses that coupling the second and fourth sets of terminals 16 and 42 with the second type of connector 14 comprises an interposer (col.6: 4-14 and 22-28).

As to Claim 16 (depending from either one of *Rejection #1* and *Rejection #2* of base Claim 9, above), Hernandez et al. further discloses that coupling the second and fourth sets of terminals 16 and 42 with the second type of connector 14 (col.6: 4-14 and 22-28) comprises physically compressing the IC package and the substrate together:

Hernandez et al. discloses that the assembly of Figs. 1 and 12 further comprises an element (i.e., a clamping frame), not shown in the Figures, to physically compress IC package 10, connector 14 and substrate 12 together to couple the IC package 10 to substrate 12 (col.6: 14-25). As indicated in col.6: 14-25, Hernandez et al. includes, but does not show, the clamping frame as part of the structure of Figs. 1 and 12, wherein the contemplated clamping frame is the one shown and described in the US Patent 4,793,814 to Zifcak et al. incorporated by reference in col.5: 33-41 of Hernandez et al. In the incorporated Zifcak et al., see the referenced clamping frame 18 compressing the package assembly 10 in Figs. 2-4 and read col.3: 5-7 and col.4: 16-28 of the incorporated Zifcak et al.). [*Examiner's Note*: Zifcak et al. is incorporated into the disclosure of Hernandez et al. and thereby enables the disclosure by providing the clamping frame element in Hernandez et al. which is not explicitly depicted in the Figures of Hernandez et al. Therefore Zifcak et al. is introduced as a secondary reference in the instant 35 USC § 102(b) rejection of Claim 16 under the provision for such multiple reference rejections given in the MPEP § 2131.01, section I].

As to Claim 31 (*Rejection #1*): Hernandez et al. discloses a IC package 10 comprising first and second sets of terminals 136 and 16, respectively, in first and second zones of a surface 18 of IC package 10, wherein first zone is labeled with element number 20 (Figs. 1, 1A and 12; col.5: 42-43; col.9: 19-23); a substrate 12 comprising third and fourth sets of terminals 140 and 42, respectively (Figs. 1 and 12; col.5: 64-66; col.9: 24-30); a first type of connector 134 to couple the first and third sets of terminals 136 and 140 (Fig. 12; col.9: 19-26); and a second type of connector 14 to

couple the second and fourth sets of terminals 16 and 42 (Figs. 1 and 12; col.6: 4-14 and 19-25).

As to Claim 31 (*Rejection #2*): Hernandez et al. discloses a IC package 10 comprising first and second sets of terminals 136 and 16, respectively of a surface 18 of package 10, wherein first zone is labeled with element number 20 (Figs. 1, 1A and 12; col.5: 42-43; col.9: 19-23); a substrate 12 comprising third and fourth sets of terminals 142/144 (via feed holes 142 in conjunction with associated vias 144; col.9: 24-26) and 42, respectively (Figs. 1 and 12; col.5: 64-66; col.9: 24-30); a first type of connector 134/140 (pins 134 in conjunction with associated sockets 140; col.9: 24-28) to couple the first and third sets of terminals 136 and 142/144 (Fig. 12; col.9: 19-28); and a second type of connector 14 to couple the second and fourth sets of terminals 16 and 42 (Figs. 1 and 12; col.6: 4-14 and 19-25).

As to Claim 32 (depending from *Rejection #2* of base Claim 31, above): Hernandez et al. further discloses that the first zone 20 is centrally located on the surface 18, and the first type of connector 134/140 comprises solder (Figs. 1A and 12; col.9: 27-30).

As to Claim 34 (depending from either one of *Rejection #1* and *Rejection #2* of base Claim 31, above), Hernandez et al. further discloses that the second type of connector 14 is an interposer (col.6: 4-14 and 22-28).

As to Claim 35 (depending from either one of *Rejection #1* and *Rejection #2* of base Claim 31, above), Hernandez et al. further discloses that the second type of connector 14 is an interposer (col.6: 4-14 and 22-28) and the assembly of Figs. 1 and

12 further comprises an element (i.e., a clamping frame), not shown in the Figures, to physically compress IC package 10, connector (interposer) 14 and substrate 12 together to couple the IC package 10 to substrate 12 (col.6: 14-25). As indicated in col.6: 14-25, Hernandez et al. includes, but does not show, the clamping frame as part of the structure of Figs. 1 and 12, wherein the contemplated clamping frame is the one shown and described in the US Patent 4,793,814 to Zifcak et al. incorporated by reference in col.5: 33-41 of Hernandez et al. In the incorporated Zifcak et al., see the referenced clamping frame 18 compressing the package assembly 10 in Figs. 2-4 and read col.3: 5-7 and col.4: 16-28 of the incorporated Zifcak et al.). [*Examiner's Note*: Zifcak et al. is incorporated into the disclosure of Hernandez et al. and thereby enables the disclosure by providing the clamping frame element in Hernandez et al. which is not explicitly depicted in the Figures of Hernandez et al. Therefore Zifcak et al. is introduced as a secondary reference in the instant 35 USC § 102(b) rejection of Claim 35 under the provision for such multiple reference rejections given in the MPEP § 2131.01, section I].

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 39 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grieco et al. in view of Dockerty et al. **(US 5,796,169)**.

As to Claim 39:

I. Grieco et al. discloses a bus coupling components in the data processing system 100; and a processor die 110 coupled to the bus (Fig. 1; col.3: 1-7 and 21).

II. Grieco et al. does not teach that the processor 110 includes at least one electronic package comprising: a die comprising first and second sets of terminals disposed in first and second zones, respectively, of a surface of the die; a substrate comprising third and fourth sets of terminals; a first type of connector to couple the first and third sets of terminals; and a second type of connector to couple the second and fourth sets of terminals.

III. Dockerty et al. discloses a processor die 3 (Fig. 4; col.3: 23-26; col.4: 36-38; col.1: 36-40 and col.5: 16-19) comprising first and second sets of terminals 4 and 15 disposed in first and second zones (second zone is labeled as 14), respectively, of a surface of die 3 (Figs. 3 and 4); a substrate comprising third and fourth sets of terminals 2 and 34, respectively, of a substrate (said substrate not shown but having connector configuration similar to that of substrate 1 in the IC package mounting embodiment of Fig. 5); a first type of connector 11 to couple the first and third sets of terminals 4 and 2; and a second type of connector 16, 18 (i.e., a "support solder") to couple the second and fourth sets of terminals 15 and 34 (Figs. 3 and 4; the coupling of IC 3 to a substrate is not shown but is similar to the coupling of IC package 24--having the same type of connector configuration as IC 3--to substrate 1 in Fig. 5). Dockerty et al. further discloses that the purpose of this structure is to selectively match high power output

locations (i.e., localized "hot spots") on the processor die 3, and supply power, provide ground lines or convey signals to and from processor die 3 (col.5: 16-24).

IV. Since Grieco et al. includes a conventional processor die in the disclosed data processing system, and the IC processor die of Grieco et al. exhibits "hot spots" which are well-known in conventional processors, as taught by Dockerty et al., then the power dissipation and power propagation benefits of the connector structure of the processor die, as taught by Dockerty et al., would have been readily recognized as beneficial to the performance and reliability of the data processing system in the pertinent art of Grieco et al. and therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the conventional processor die of Grieco et al. with the processor die of Dockerty et al. in order to enhance the power dissipation capabilities of the processor die in the processor of Grieco et al., as taught by Dockerty et al., and thereby improve reliability and performance of the data processing system of Grieco et al.

As to Claim 42, Grieco et al. further discloses a display coupled to the bus and an external memory coupled to the bus (Fig. 1; col.3: 7-10).

Allowable Subject Matter

9. Claims 3, 6-8, 14, 19, 22-26, 28-30, 33, 37, 38, 40 and 41 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sathe et al. (US 2002/0065965 A1: *pre-grant publication of US Application No. 09/726,629 cited as a related Application on p.1, lines 8-11 of Applicant's Specification*) discloses an IC or IC package electrically connected to a substrate by means of an interposer having holes filled with electrically conductive elements (ECE) 124, said ECEs 124 comprising cylindrical or hour-glass shaped wads of conductive, elastic metal wire (Figs. 5-8, 16 and 17; p.4, paragraph [0056]).

Gaudenzi et al. (US 5,490,040) discloses a package substrate 54 having solder balls 56 in a central zone and pins 58 in a peripheral zone for mounting onto circuit card 60 (Figs. 6-8).

Tanizawa (US 5,475,261) discloses a package substrate with first connectors (71, 81, 91) in a central zone and second connectors 14 in a peripheral zone (Figs. 7A,B, 8A,B and 9A,B), wherein the central zone connectors have larger cross-sectional areas for carrying power/ground signals (Figs. 3D, 4 and 5; col.3: 15-24).

Hayes et al. (US 6,463,493 B1) discloses a data processing system 120 having a processor (CPU) display and external memory coupled to the bus 232 (Fig. 2; col.4: 18-45).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

John B. Vigushin
Examiner
Art Unit 2827

jbv
April 2, 2003